REMARKS

Claims 1-16 and 90 are pending in the present application. In the Office Action dated April 28, 2006, claims 1-2, 7 and 9 were rejected under 35 U.S.C. 102(e) as being anticipated by Alexander et al. (U.S. Patent No. 6,798,666) ("Alexander"). Claims 3-6 were rejected under 35 U.S.C. 103(a) as being unpatentable over "Alexander" in view of Haley (U.S. Patent No. 5,006,962) ("Haley"). Claims 8 and 10 were rejected under 35 U.S.C. 103(a) as being unpatenable over "Alexander" in view of Admitted Prior Art. Claims 1-16 were rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-16 of U.S. Patent No. 6,922,341. Claims 1-16 were provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 49-64 of co-pending Application No. 11/041,106. Claims 1-16 were provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 17-32 of co-pending Application No. 11/040,575.

The embodiments disclosed in the present application will now be discussed in comparison to the cited references. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the cited references, does not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

Anticipated Under 35 U.S.C. 102(e)

The present application is directed to electronic module packages having a capacitor incorporated within the package for coupling signals between the modules while causing the modules to be isolated from each other for direct current ("DC"). The purpose of electrically isolating the modules is to prevent the direct current flow in a serial bus from causing signal degradation and damage to the circuitry. The IEEE 1394 documents suggests using an external capacitor and resistor to isolate modules; however, that creates large and bulky devices. In the disclosed embodiment, a capacitor formed by first and second conductive surfaces is incorporated within the package.

In one embodiment, as shown in Figure 3 of the present application, the structure includes a first and second module attached to the first side of a substrate. A capacitor is formed

within the package by conductively coupling the ground plane of the first electronic module 304 to a first conductive surface 310 below the substrate 302; and conductively coupling the ground plane of the second electronic module 305 to a second conductive surface 312, which is spaced apart from the first conductive surface 310. As a result, the first and second modules are capacitively coupled to each other. The first electronic module 304 is conductively coupled to the first conductive surface and isolated from the second conductive surface 312, and the second electronic module 305 is conductively coupled to the second conductive surface and isolated from the first conductive surface 310. If the first electronic module 304 was not isolated from the second conductive surface then the first electronic module 304 would not be capacitively coupled to the second electronic module 305 since the second electronic module 305 is conductively coupled to the second conductive surface. Similarly, if the second electronic module 305 was not isolated from the first conductive surface then the second electronic module 305 would not be capacitively coupled to the first electronic module 304 since the first electronic module 304 is conductively coupled to the first conductive surface.

The Examiner has cited the Alexander reference. The Alexander reference is directed toward mitigating the effects of noise and electromagnetic interference (EMI) in a multilayer PCB by introducing a loss in the current path. In order to reduce the effects of noise and EMI, the Alexander reference employs a resistor connected in series with a decoupling capacitor. Figure 2 in the Alexander reference discloses a multi-layer PCB 120 with an additional loss element between power and ground. Figure 2 further shows a decoupling capacitor 160 module and a resistor-capacitor pair 180 module on a conductive layer 135. The decoupling capacitor 160 module and a resistor-capacitor pair 180 module each have a pair of leads that are connected to first and second conductive surfaces 125, 130, respectively, which form a capacitor. The Alexander reference does not disclose integrated circuits modules. The Examiner apparently contends the decoupling capacitor and resistor-capacitor pair modules correspond to applicant's first and second electronic modules 304, 305. However, since each of these modules is connected to both the first conductive surfaces 125 and the second conductive surfaces 130, and neither is isolated from the first conductive surfaces 125 or the second conductive surfaces 130, the capacitor formed by the surfaces 125 and 130 cannot capacitively couple the decoupling capacitor 160 module to the resistor-capacitor pair 180 module.

Turning now to the claims, the patentably distinct differences between the cited references and the claim language will be specifically pointed out. Presently amended claim 1 recites, in part, "a first conductive surface proximate to the second side of the substrate, the first module conductively coupled to the first conductive surface and *isolated from the second conductive surface;* a second conductive surface spaced apart from the first conductive surface to form a capacitor with the first conductive surface, the second module conductively coupled to the second conductive surface and *isolated from the first conductive surface.*" (Emphasis Added). The Alexander reference does not disclose or fairly suggest the above limitation. Rather, the Alexander reference discloses a decoupling capacitor 160 module conductively coupled to *both* the first conductive surface 125 *and* the second conductive surface 130. Similarly, the resistor-capacitor pair 180 module is conductively coupled to *both* the first conductive surface *and* the second conductive surface 130. (Emphasis Added). In contrast, claim 1 indicates that the first module is isolated from the second conductive surface and the second module is isolated from the first conductive surface. Therefore, presently amended independent claim 1 is allowable over the Alexander reference.

New independent claim 90 recites, in part, "a first *integrated circuit module* attached to the first side of the substrate; a second *integrated circuit module* attached to the first side of the substrate." (Emphasis Added). The Alexander reference does not disclose or fairly suggest the above limitation. Rather, the Alexander reference discloses a decoupling capacitor 160 module and a resistor-capacitor pair 180. In contrast, claim 90 indicates that the modules are integrated circuits. Therefore, new independent claim 90 is allowable over the Alexander reference.

The claims depending from the above-discussed independent claims are also patentable because of their dependency from patentable independent claims and because of the additional limitations recited in the dependent claims.

Obviousness-type Double Patenting Rejection

With regard to the obviousness-type double patenting rejection, applicants are filing a terminal disclaimer in order to obviate it. Accordingly, the multiple double patenting rejections should be withdrawn.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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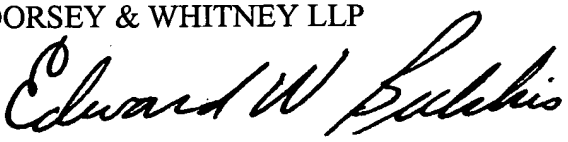

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